WE CLAIM:

1. In a radio frequency (RF) receiver having an analog gain control section for controlling the gain of a received RF signal, and a digital demodulator section for demodulating the output of the gain control section, the improvement comprising:

an analog GO circuit connected to recognize the presence of a data packet within a received RF signal in said analog gain control section, and in response to produce an analog GO signal,

a digital GO circuit connected to recognize the presence of a data packet within said received RF signal from said digital demodulator section, and in response to produce a digital GO signal, and

control circuitry connected to enable gain control functions within said analog gain control section and digital demodulator functions within said digital demodulator section in response to respective analog and digital GO signals.

2. The RF receiver of claim 1, wherein said control circuitry enables said digital demodulator functions in response to both analog and digital GO signals.

3. The RF receiver of claim 1, wherein said control circuitry enables said gain control functions only in response to an analog GO signal.

4. The RF receiver of claim 3, wherein said control circuiting enables said digital demodulator functions in response to either an analog or a digital GO signal.

5. The RF receiver of claim 1, wherein said analog GO circuit recognizes the presence of a data packet by sensing the power of said RF signal.

6. The RF receiver of claim 5, wherein said analog GO circuit distinguishes a data packet from noise and co-channel interference, but not adjacent channel interference.

7. The RF receiver of claim 6, wherein said digital GO circuit distinguishes a data packet from adjacent channel interference, but not co-channel interference.

8. The RF receiver of claim 1, wherein said digital GO circuit recognizes the presence of a data packet by sensing the energy of said RF signal.

9. The RF receiver of claim 8, wherein said digital GO circuit distinguishes a data packet from adjacent channel interference, but not co-channel interference.

10. The RF receiver of claim 9, wherein said digital GO circuit includes FIR filters which attenuate adjacent channel interference sufficiently for said digital GO circuit to distinguish a data packet from adjacent channel interference.

11. The RF receiver of claim 1, wherein said analog gain control section includes a received signal strength indicator (RSSI) and an analog-to-digital converter connected to digitize the output of said RSSI, and the remainder of said analog gain control circuit operates in the digital domain based upon said digitized RSSI output.

12. The RF receiver of claim 1, for use with RF signals comprising data packets having a limited-bit preamble, wherein said analog and digital GO circuits recognize the presence of a preamble as an indication of the presence of a data packet, and in response produce said analog and digital GO signals.

13. The RF receiver of claim 1, further comprising circuitry for converting a received RF signal to digital format with a sample rate greater than the data packet bit rate, and a symbol timing recovery (STR) circuit that identifies those periodic samples of the preamble portion of a data packet which are spaced by the bit period and most closely match the preamble bits, said receiver employing a continuation of said identified periodic samples to decode the remainder of said data packet.

14. The RF receiver of claim 13, said STR circuit comprising a plurality of accumulators equal in number to the ratio of said sample rate to the data packet bit rate, said accumulators cross-correlating successive respective preamble samples with the bits represented by said samples, and a selector for selecting the accumulator which yields the greatest cross-correlation as the source of samples to decode the remainder of said data packet.

15. The RF receiver of claim 14, wherein said selector makes its selection based upon the highest absolute value of cross-correlation.

16. The RF receiver of claim 13, wherein said STR circuit is enabled in response to a GO signal.

17. The RF receiver of claim 16, wherein said STR circuit is enabled in response to both an analog and a digital GO signal.

18. An analog gain control circuit for a radio frequency (RF) receiver, comprising:

an RF input terminal,

gain control circuitry connected to control the gain of an RF signal at said input terminal,

a received signal strength indicator (RSSI) connected to sense the strength of an RF signal in said gain control circuitry,

first and second propagation paths connected to impart different delays to the output of said RSSI,

an offset circuit connected to adjust the differential in signal levels between the outputs of said paths, and

a GO signal generator connected to produce a first GO signal in response to said adjusted signal differential exceeding a threshold level, said first GO signal being employed to enable gain control functions within said gain control circuitry.

19. The gain control circuit of claim 18, wherein said first propagation path imparts a zero intentional delay.

20. The gain control circuit of claim 18, wherein said second path imparts a greater delay than said first path, said offset circuit amplifies the signal level in said second path, and said GO signal generator compares the difference between the outputs of said first and second paths to said threshold level.

21. The gain control circuit of claim 20, wherein said offset circuit amplifies the signal level in said second path by a gain factor that is selected based upon the signal-to-noise ratio (SNR) of a received RF signal.

22. The gain control circuit of claim 21, for RF signals where SNR is a function of RF signal level, said offset circuit including adjustment circuitry connected to dynamically adjust said gain factor based upon the level of a received RF signal.

23. The gain control circuit of claim 18, wherein said first and second propagation paths include respective integrators connected to integrate the signals in said paths over a predetermined integration period, said GO signal generator producing said first GO signal in response to said integrated signals.

24. The gain control circuit of claim 23, wherein said second path includes a signal delay that exceeds the first path delay by at least said integration period.

25. The gain control circuit of claim 24, wherein said second path signal delay exceeds the first path delay by at least the sum of said integration period and the rise time of said RSSI.

26. The gain control circuit of claim 18, for an RF signal comprising a data packet with a multiple-bit preamble of alternating bit polarities, wherein the difference between the delays of said first and second paths is at least equal to the period of said preamble.

27. The gain control circuit of claim 18, further comprising an analog-to-digital converter (ADC) connected to digitize the output of said RSSI; said propagation paths, offset circuit and GO signal generator operating in the digital domain.

28. The gain control circuit of claim 27, said gain control circuitry including a voltage gain amplifier (VGA), with the output of said ADC connected to control the gain of said VGA.

29. The gain control circuit of claim 28, said gain control circuit including a low noise amplifier (LNA) and downconverting mixer upstream of said VGA, further comprising a combining circuit connected to combine the output of said ADC with the gain differential between said LNA and mixer, and in response to produce a gain setting output for said LNA and mixer.

30. The gain control circuit of claim 18, further comprising:

an analog-to-digital converter connected to produce a digitized output from said gain control circuitry,

a digital demodulator section connected to demodulate said digitized output,

third and fourth propagation paths connected to impart different delays to said digitized output, and

a digital GO signal generator connected to produce a digital GO signal in response to the difference between said delayed signals exceeding a threshold level, said digital GO signal being employed to enable digital demodulator functions within said digital demodulator section.

31. The gain control circuit of claim 30, wherein said first GO signal is also employed to enable said digital demodulator functions.

32. The gain control circuit of claim 30, further comprising at lease one FIR filter connected prior to said third and fourth propagation paths to attenuate adjacent channel interference in said digitized output.

33. The gain control circuit of claim 30, wherein said third and fourth propagation paths include both in-phase and quadrature components.

34. In a radio frequency (RF) receiver that includes gain control circuitry connected to control the gain of a received RF signal, an analog-to-digital converter (ADC) connected to produce a digitized output from said gain control circuitry, and a digital demodulator section for demodulating the output of said ADC, the improvement comprising:

a pair of propagation paths connected to impart different delays to said digitized output, and

a digital GO signal generator connected to produce a digital GO signal in response to the difference between said delayed signals exceeding a threshold level, said digital GO signal being employed to enable digital demodulator functions within said digital demodulator section.

35. The RF receiver of claim 34, further comprising at least one FIR filter connected prior to said propagation paths to attenuate adjacent channel interference in said digitized output.

36. The RF receiver of claim 35, wherein said propagation paths include both in-phase and quadrature components.

37. The RF receiver of claim 34, wherein one of said propagation paths imparts a zero intentional delay.

38. In a radio frequency (RF) receiver for RF data packets having a preamble with a defined bit pattern, said receiver including circuitry for converting a received RF signal to digital format with a sample rate greater than the data packet bit rate, and circuitry for recognizing the preamble of a received data packet, the improvement comprising:

a symbol timing recovery (STR) circuit that identifies those periodic samples of the preamble of a received data packet that are spaced by the bit period and most closely match the preamble bits,

said receiver employing a continuation of said identified periodic samples to decode the remainder of said data packet.

39. The RF receiver of claim 38, said STR circuit comprising a plurality of accumulators equal in number to the ratio of said sample rate to the data packet bit rate, said accumulators cross-correlating successive respective preamble samples with the bits represented by said samples, and a selector for selecting the accumulator which yields the greatest cross-correlation as the source of samples to decode the remainder of said data packet.

40. The RF receiver of claim 39, wherein said selector makes its selection based upon the highest absolute value of cross-correlation.

41. The RF receiver of claim 38, wherein said STR circuit is enabled in response to the recognition of the preamble of a received data packet.

42. A method of receiving a data packet within a received radio frequency (RF) signal, in an RF receiver that includes an analog gain control section for controlling the gain of a received RF signal, and a digital demodulator section for demodulating the output of the gain control section, comprising:

enabling gain control functions within said analog gain control section in response to the recognition of a data packet in said gain control section, and

enabling digital demodulator functions within said digital demodulator section in response to the recognition of a data packet in said digital demodulator section.

43. The method of claim 42, further comprising enabling said digital demodulator functions in response to the recognition of a data packet in said gain control section.

44. The method of claim 42, wherein a data packet is distinguished from noise and co-channel interference, but not adjacent channel interference, in said gain control section.

45. The method of claim 43, wherein a data packet is distinguished from adjacent channel interference in said digital demodulator.

46. The method of claim 42, wherein a data packet is recognized in said gain control section by comparing a preamble to said data packet with a delayed portion of said received signal.

47. The method of claim 46, further comprising amplifying said delayed received signal portion prior to said comparison.

48. The method of claim 46, wherein said preamble and delayed received signal portion are integrated prior to said comparison.

49. The method of claim 46, wherein a received signal strength indication of said received signal is obtained, and said preamble and delayed received signal portion are obtained from said received signal strength indication.

50. The method of claim 42, wherein a data packet is recognized in said digital demodulator section by comparing a preamble to said data packet with a delayed portion of said received signal.

51. The method of claim 50, wherein said comparison is performed between both in-phase and quadrature components of said preamble and delayed portion of said received signal.

52. The method of claim 50, wherein said preamble and delayed portion of said received signal are integrated prior to said comparison.

53. The method of claim 50, further comprising attenuating adjacent channel components of said received signal in said digital demodulator section prior to said comparison.

54. The method of claim 42, further comprising converting a received RF signal to digital format for said digital demodulator section with a sample rate greater than the data packet bit rate of a received RF signal, wherein one of said demodulator functions comprises identifying those periodic samples of the preamble of a received data packet that that are spaced by the bit period and most closely match the preamble bits, and employing a continuation of said identified periodic samples to decode the remainder of said data packet.

55. The method of claim 54, wherein said periodic samples are identified by cross-correlating successive respective preamble samples with the bits represented by said samples, and selecting the samples with the grestest cross-correlation.

56. The method of claim 55, wherein the samples with the highest absolute value of cross-correlation are selected.